Fast Magnet Current Change Monitor (FMCM)

User's Short Manual

Version of this manual: V 0.1

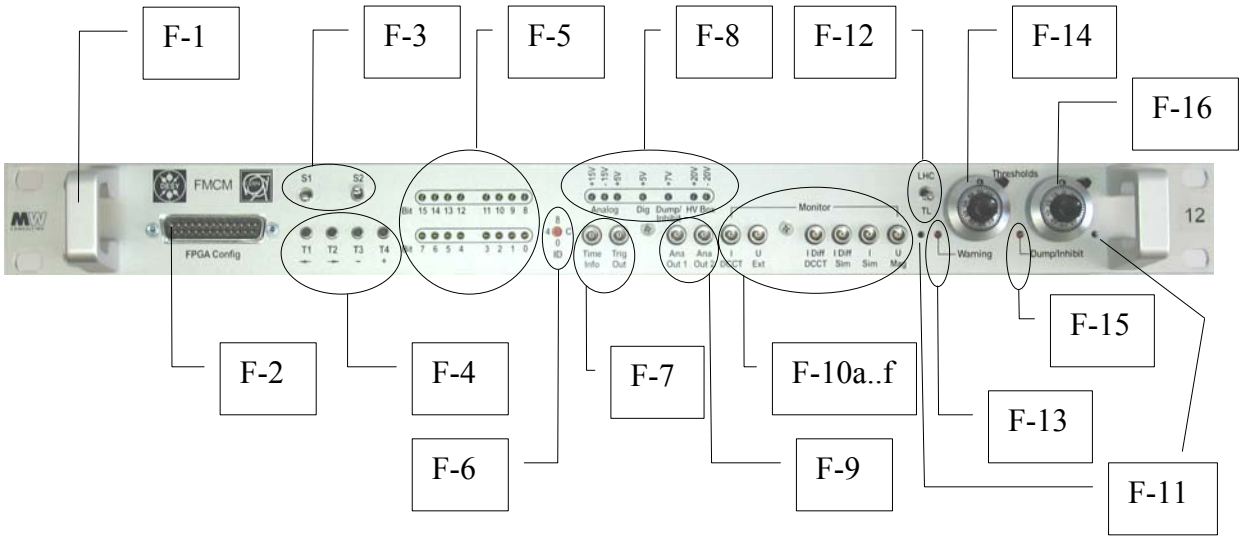
Referenced firmware version: V_10

Date: 31 July 2007

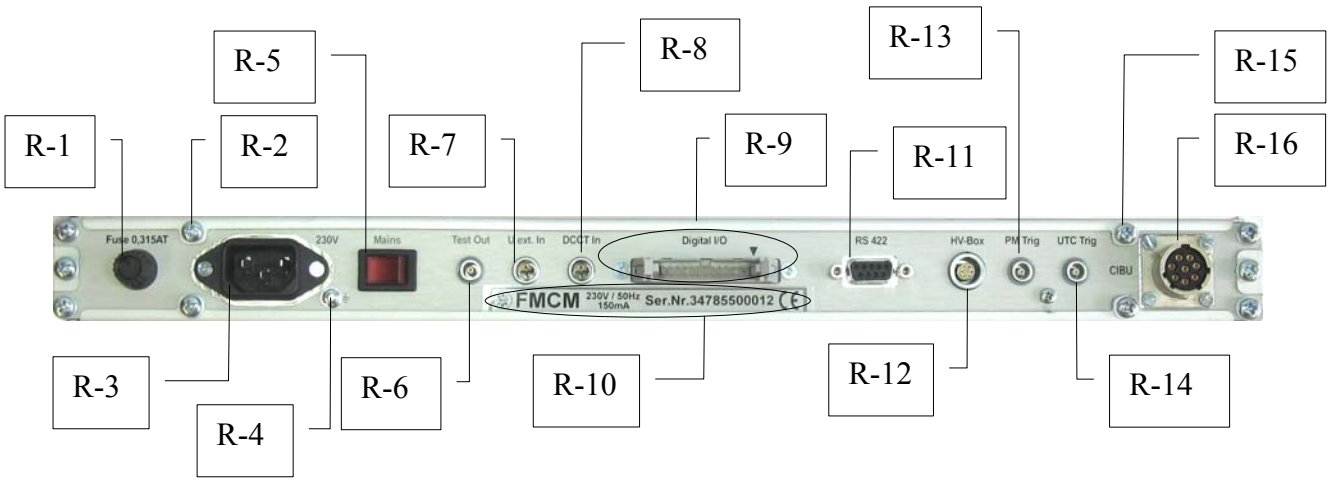
General Warning hints

- Only qualified personnel may open the device.
- Pull the power plug before opening the device.
- The device may only be used for the purpose described in this manual.
- Use handles [F-1] to insert and pull out the device.
- The device complies with protection class IP-30.
- The device is not permitted for safeguarding of persons
- Application of a voltage above 42V is not permitted at any terminal (except Mains plug [R-3]). Read warning hints for connector [R-12] on page 9
- This manual replaces all previous versions.

Front panel (without protection cover), see page 6:



Rear panel, see page 8:



Common specifications

Power requirement: 230V~ 50Hz 150mA
Operating temperature range: +5 to +35°C

Glossary

"EGND":	Electronic ground in the device. Connected via a 100 Ω resistor to PE.
FPGA:	Field Programmable Gate Array: the programmable control unit of the device.
PE:	Protection Earth: Pin of the mains plug [R-3] which is connected to the case.

Scope of this manual

This manual covers

- Warning hints
- Operation and hardware specifications of external controls and connectors
- Default operation principle for LHC and the Transfer Lines

This manual does not cover

- The RS422 remote control protocol
- Test procedures
- Service and calibration procedures
- Special firmware functionality
- Functionality of switches inside the case
- Functionality of firmware driven LEDs [F-5] – for more information, see firmware description

This manual describes mainly hardware features. If functionality depends on the firmware, this is written expressly.

Default device operation principle

Undesired magnet current changes in the LHC accelerator or in Transfer Lines can cause severe damage by particles hitting the vacuum chamber or other components. The FMCM is designed to detect such changes as fast as possible to generate an alarm which results in a beam dump (for the LHC) or beam inhibit (for Transfer Lines). On the other hand, undesired dumps by noise or electrical interference have to be reduced to a minimum.

The voltage of a magnet in the accelerator is fed to a so-called "HV-Box" containing a voltage divider and an isolation amplifier. The downscaled and isolated signal from the "HV-Box" is connected to the input connector [R-12] of the FMCM. The FMCM uses the signal to calculate a signal corresponding principally to the magnet current change. If the calculated

change exceeds a value set by the threshold potentiometer [F-16], an alarm is given to connector [R-16] by switching the output voltage from >5V to 0V.

Hints for reliable protection operation

- Make sure to apply the correct polarity for the magnet voltage at input [R-12], otherwise no dumps will be generated.
- For standard operation be sure that the Dump/Inhibit potentiometer [F-16] and the LHC/TL switch [F-12] are in correct position and use the protection cover to avoid unintended changing of the settings.
- For standard operation be sure that Jumper ST3 on the mainboard is connected to use the hardware redundancy feature.
- Note that the device only detects fast changes. Slow changes or derivations of the desired magnet current must be supervised by other equipment. Make sure that for any change rate of the magnet current dangerous states are excluded.
- The calibration of the device has to be tested once per year; in case of especial stress more often.
- The electrolytical capacitors should be replaced after each 10 years of operation.

Important application hints

- Connection of grounded devices to the FPGA Config connector [F-2], to the digital outputs [F-7], to the analog outputs [F-9], to the monitor outputs [F-10], to the Test output [R-6] or to the Digital I/O connector [R-9] can affect operation due to ground loops, especially if several devices with different ground potential are connected at the same time or if the ground potential of the connected devices is different from PE or different from the ground of the "CIBU" device connected to [R-16].
    - → If an oscilloscope is connected to one or more of the Lemo connectors of the device, no grounded computer should be connected to the FPGA Config connector [F-2] to avoid inaccurate oscilloscope readings due to ground loops.
- Avoid manipulations at the device (connecting or disconnecting devices, change of the setting of operating controls) during beam is stored to avoid unwanted beam loss. If manipulations are essential, devices to be connected should be discharged and persons should discharge themselves to prevent unwanted alarms due to electrostatical discharge (ESD).
- Put ESD protection covers on the connectors "FPGA Config" [F-2] and "Digital I/O" [R-9] while these connectors are not used to prevent damage and malfunction.
- If the connector "Digital I/O" [R-9] is used, observe the common ESD precautions for MOS devices because some of the pins of [R-9] are connected directly to FPGA pins without further ESD protection.
- **Do not operate the device close to devices with high temperature and do not cover the ventilation slots to admit free air circulation – otherwise lifetime can be reduced.**

Freewheeling diode selection

The default operation mode of the magnets is with freewheeling diodes. In this case the magnet voltage cannot go negative – it will be “unipolar”.
For some magnets freewheeling diodes cannot be used and the magnet voltage can become negative while the magnet is ramped down or switched off – the magnet voltage will be “bipolar”.
For optimum resolution of the built-in 12-bit-ADC, the full range of the ADC can be switched between 0V to 10V (unipolar) and -10V to 10V (bipolar) with an analog switch controlled by the FPGA.
In FPGA firmware version V_10, the selection is done by switch x of the “PARAM” DIP switch on the mainboard:

PARAM switch 6 = OFF (default)	unipolar magnet voltage (with freewheeling diodes)
PARAM switch 6 = ON	bipolar magnet voltage (without freewheeling diodes)

In firmware version V_10, the ADC values are not used to generate alarms, so the selection is not relevant for the dump or beam inhibit functionality, only for the post mortem recording.

Front panel connectors and control elements, see page 2

[F-1] Handle

[F-2] Connector „FPGA Config.“ (25-pin DSUB):
For configuration of the FPGA and for programming the configuration EEPROM; to be connected to the LPT connector of a personal computer running ALTERA PROGRAMMER software.

[F-3] Switches “S1” and “S2”:
Connected only to FPGA inputs, function depends on FPGA firmware.

[F-4] Pushbuttons “T1”, “T2”, “T3” and “T4”:
Connected only to FPGA inputs, function depends on FPGA firmware.

[F-5] 16 LEDs: “0” to “15”
Connected only to FPGA outputs, function depends on FPGA firmware. Mainly used to display data and status information, depending on the position of the hex switch [F-6] and in some cases depending on the position of the switches [F-3] and on pressing of the pushbuttons [F-4].

[F-6] Hex switch:
Switch with 16 hexadecimal positions (0 to 9 and A to F), to be operated by a screwdriver.
Connected only to FPGA inputs, function depends on FPGA firmware.
Normally used to select test modes, the display mode of LEDs [F-5] and the functionality of the outputs [F-7] and [F-9] and connector [R-9].

[F-7] Lemo connectors “Time Info” and “Trig Out” (digital outputs):
Low impedance TTL compatible digital outputs driven by FPGA outputs, function depends on FPGA firmware and on switch [F-6]
Low = approx. 0V, High = approx. 5V
Output impedance: typ. 31 Ω for “High”, typ. 13 Ω for “Low”
The outputs can directly drive the inputs [R-13] or [R-14].
Typical applications: oscilloscope trigger for display of recorded waveforms from outputs [F-9], permit signal monitor, test signals for inputs [R-13] or [R-14].

[F-8] Power supply LEDs:
Show operation of the built-in power supplies. All LEDs must be illuminated when the device is powered.

[F-9] Lemo connectors “Ana Out 1” and “Ana Out 2” (analog outputs):
multi-purpose analog outputs driven by individual 12-bit-DACs which are controlled by the FPGA.
Function depends on FPGA firmware and on switch [F-6].
Voltage range: 0V to 4.191V, Output impedance approx. 5 kΩ

[F-10a..f] 6 Lemo connectors for analog monitoring of certain signals:

a) “I DCCT”: monitor the signal of input [R-8]. Defined output voltage range: 0 to 10V (if signal at “DCCT In” [R-8] is in the defined voltage range 0 to 10V).
b) “U Ext”: monitor the signal of input [R-7].

c) "I Diff DCCT": monitor the signal of input [R-8] after amplification and differentiation (to eliminate the constant signal component); the time constant of the differentiation depends on switch [R-12].
d) "I Diff Sim": monitor the signal of the magnet voltage input pins of [R-12] after integration (to simulate the magnet current from the magnet voltage for a certain time constant), amplification and differentiation (to eliminate the constant signal component). The time constants of integration and differentiation both depend on switch [F-12].
e) "I Sim": monitor the signal of the magnet voltage input pins of [R-12] after integration (to simulate the magnet current from the magnet voltage for a certain time constant). The integration time constant depends on switch [F-12].
f) "U Mag": monitor the signal of the magnet voltage input pins of [R-12]. Defined output voltage range: 0 to 10V in unipolar mode and -10V to +10V in bipolar mode. Selection of mode unipolar/bipolar is controlled by FPGA firmware – see chapter "Freewheeling diode selection".

The output impedance of [F-10a..f] is approx. 2 kΩ
The defined output voltage range for [F-10**b..e**] is -10V to 10V
If signal at "DCCT In" [R-8] is in the defined voltage range (0 to 10V), the voltage range at "I DCCT" [F-10a] will also be in this voltage range. For negative voltages, the corresponding ADC channel will show overflow (for firmware version V_10 only relevant for the post mortem recording).

[F-11] 2 tap holes to fix the protection cover

[F-12] switch "LHC/TL"
Mode selection: "LHC" for storage ring operation, "TL" for transfer line operation
The time constants for the integration in the magnet voltage signal path and the differentiation in the magnet voltage and DCCT signal path are directly selected by this switch using analog switches. The switch also feeds an FPGA input to select the digital alarm processing and the LED functionality.

[F-13] LED "Warning":
Driven by an FPGA output, functionality depends on FPGA firmware.
Standard function: the LED is used to test the alarm threshold by changing the warning potentiometer [F-14] without changing the real threshold.

[F-14] Potentiometer for Warning threshold":
Range: 0.00 to 10.00, corresponding to a warning threshold of ±0.00V to ±10.00V for the integrated, amplified and differentiated magnet voltage seen at connector [F-10d] (normal case, Jumper ST18 in position "Umag") or for the amplified and differentiated DCCT signal seen at connector [F-10c] (special case, Jumper ST18 in position "DCCT").
This potentiometer acts only on the Warning LED [F-13].

[F-15] LED "Dump/Inhibit":
Driven by an FPGA output, functionality depends on FPGA firmware.
Normal function: if switch [F-12] is in position "LHC", the LED flashes if an alarm is generated. If switch [F-12] is in position "TL", the LED flashes if an alarm is active while a trigger signal occurs at trigger input "PM Trig" [R-13].

[F-16] Potentiometer for Dump/Inhibit threshold":
Range: 0.00 to 10.00, corresponding to a Dump/Inhibit threshold of ±0.00V to ±10.00V for the integrated, amplified and differentiated magnet voltage seen at connector [F-10d] (normal case, Jumper ST18 in position "Umag") or for the amplified and differentiated DCCT signal seen at connector [F-10c] (special case, Jumper ST18 in position "DCCT").
This potentiometer acts on the Dump/Inhibit LED [F-15] and on the alarm output [R-16]: the permit signals change from >5V to approx. 0V if the threshold is exceeded.

Rear panel connectors and control elements, see page 2

[R-1] Fuse for Mains power 230V: 0.315A T

[R-2] (and [R-15]): Screws to remove the cover to access the mainboard
Open only these screws to access the elements on the mainboard!

[R-3] Mains plug 230V~

[R-4] PE screw: **Do not unscrew!**

[R-5] Mains 230V switch, alluminated if switched ON

[R-6] Lemo connector "Test Out":
Output for analog test signals, driven by the FPGA via a12-bit-DAC.
Voltage range: -11V to +11V (calibrated)
Output impedance: 2 kΩ

[R-7] 2-pin Lemo connector "U ext In":
Differential multi-purpose analog input.
Pin 1: In+ Pin 2: In- if internal Jumper ST8 is in default position "A = +"
Differential voltage range: -10V to +10V
Common mode voltage range: -12V to +12.5V
Input impedance: >1MΩ

[R-8] 2-pin Lemo connector "DCCT In":
Differential analog input for a DCCT (device to measure the magnet current).
Pin 1: In+ Pin 2: In-
Differential voltage range: 0V to +10V. Negative voltages will generate ADC overflow in the Post Mortem recorder
Common mode voltage range: -12V to +12.5V
Input impedance: >1MΩ

[R-9] 3M connector 26-pole "Digital I/O"
This connector should be used only for test applications.
For standard operation, the connector should be covered to avoid ESD damage.
Observe ESD handling precautions if the connector is not covered.
Connection of a grounded device can affect operation due to ground loops
Pinning:

- Pin 1: +5V via 0.68Ω resistor. To be used as power supply for external device (max. 100mA; not short circuit protected!) and for power supply check

- Pin 2: +7V_Dump (unstab.) via 10 kΩ resistor. (For power supply check)
- Pin 3: +15V via 10 kΩ resistor. (For power supply check)
- Pin 4: –15V via 10 kΩ resistor. (For power supply check)
- Pin 5: +5V_AN via 10 kΩ resistor. (For power supply check)
- Pins 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26: "EGND"
- Pins 7, 9, 11, 13, 15, 17, 19, 21, 23, 25: Digital I/O pins connected to FPGA, function and data direction depends on FPGA firmware and setting of Hex switch [F-6]

[R-10] Type plate with series number

[R-11] DSUB 9-pole connector "RS 422"
RS 422 input and output for remote control
Pinning: ("In" means direction from external device to FMCM)

- Pin 1: Data In +
- Pin 2: Data In –
- Pin 4: Data Out +
- Pin 5: Data Out –
- Pins 3, 6, 7, 8, 9 are connected together and connected to "EGND" via 100 Ω resistor

[R-12] 6-pin-Lemo connector "HV-Box":
Connection (up to 100m) to a high voltage box "HV-Box" containing magnet voltage divider and isolation amplifier. For a long distance connection, make sure the cable resistance for the power supply is low enough.
Pin 1, 2, 3 is a differential input to receive the magnet voltage signal from the isolation amplifier in the "HV-Box"; the outputs of the galvanically isolated power supply (pin 4, 5, 6) are designed to supply the isolation amplifier in the "HV-Box":

- Pin 1: Connected to electronic ground "EGND" via 1kΩ resistor; to be connected to the output ground of the isolation amplifier in the "HV-Box" to keep the voltages at pin 2 and pin 3 inside the common mode voltage range
- Pin 2: Magnet voltage in +
- Pin 3: Magnet voltage in –
- Pin 4: Power supply ground (without galvanic connection to electronics ground "EGND" inside the FMCM)
- Pin 5: Power supply out +20V unregulated
- Pin 6: Power supply out –20V unregulated

Differential input voltage range: 0 to 10V in unipolar mode and -10V to +10V in bipolar mode. Negative voltages in unipolar mode will generate ADC overflow in the Post Mortem recorder. Selection of mode unipolar/bipolar is controlled by FPGA firmware – see chapter "Freewheeling diode selection".
Attention: for negative magnet voltages (for mode "unipolar" or "bipolar") no beam dumps will be generated, so be sure to observe the correct polarity of the magnet voltage independently of the mode setting ("unipolar" or "bipolar")!
Common mode input voltage range: -12V to +12.5V
Input impedance: >1MΩ
WARNING: No external voltage may be connected to this connector!
The connected device must be double-fail-safe: failure of a single component (short or open) – especially at the high-voltage-divider or the isolation amplifier – must not put a voltage > 42V to any pin of this connector!

[R-13] Lemo connector “PM Trig”:
Designed for connection to a CERN Timing module output of type “CTRP” or “TG8” with the output pulse width set to 2µs
Opto isolated input to FPGA.
Typically used as input for extraction pulse or Post Mortem Trigger
Electrical Specs:

- **Input pulse specification: normally high, pulsed active low with duration 2µs**
- Cable length between Timing module and FMCM: 0 to 60m with CERN cable type “LO-GE Nº461”
- Input voltage (inner connector referenced to outer connector): 0V to 5V
- Threshold voltage: typ. 1.5V
- Voltage “Low”: <1.2V; Voltage “High”: >2.0V
- AC impedance: typ. 50Ω
- DC input current at 5V: typ. 8.2 mA
- Max. voltage between outer connector and PE: ±10 V

[R-14] Lemo connector “PM Trig”:
Designed for connection to a CERN Timing module output of type “CTRP” or “TG8” with the output pulse width set to 2µs
Opto isolated input to FPGA.
Typically used as input for “pps” pulses: 1 pulse per second
Electrical Specs: same as for [R-13], see above

[R-15] (and [R-2]) Screws to remove the cover to access the mainboard
Open only these screws to access the elements on the mainboard!

[R-16] Burndy connector 8-pole “CIBU”
Alarm output and status input
The threshold of the status input (Pin 7) is a standard TTL threshold (approx. 1.5V) referenced to “EGND”.
Two independent Permit output pairs (Permit A +, Permit A – and Permit B +, Permit B –) exist for redundancy. They supply (7V/12mA if Permit=True) or (0V if Permit=False), designed to be compatible to the specifications of the CERN CIBU Box.
Pinning:

- Pin 1: EMC Ground (connected to electronic ground “EGND” via 10Ω resistor)
- Pin 2: EMC Ground (connected directly to pin 1, see above)
- Pin 3: Permit A + (connected to 7V unstab. via 10Ω + Polyfuse 50mA)
- Pin 4: Permit A – (switched to “EGND” via 10Ω if Permit active, else open)
- Pin 5: Permit B + (connected to 7V unstab. via 10Ω + Polyfuse 50mA)
- Pin 6: Permit B – (switched to “EGND” via 10Ω if Permit active, else open)
- Pin 7: CIBU Status + (high impedance input with 4k7 pullup to 7V unstab.)
- Pin 8: CIBU Status – (connected to electronic ground “EGND” via 10Ω resistor)